Experiment No.7

Aim: To study, design and implement various synchronous counters. Also understand its practical applications.

# Objectives:

1. To understand functioning of synchronous counters.
2. To design and implement synchronous counters using various flip flops.
3. To understand timing diagram of synchronous counters and frequency calculations.
4. To understand problems associated with synchronous counters.

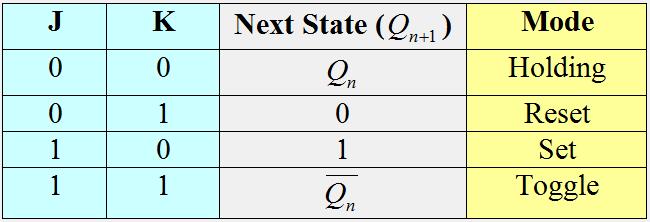
# Equipment:

IC’s, regulated power supply, bread board, connecting wires, LED, DMM.

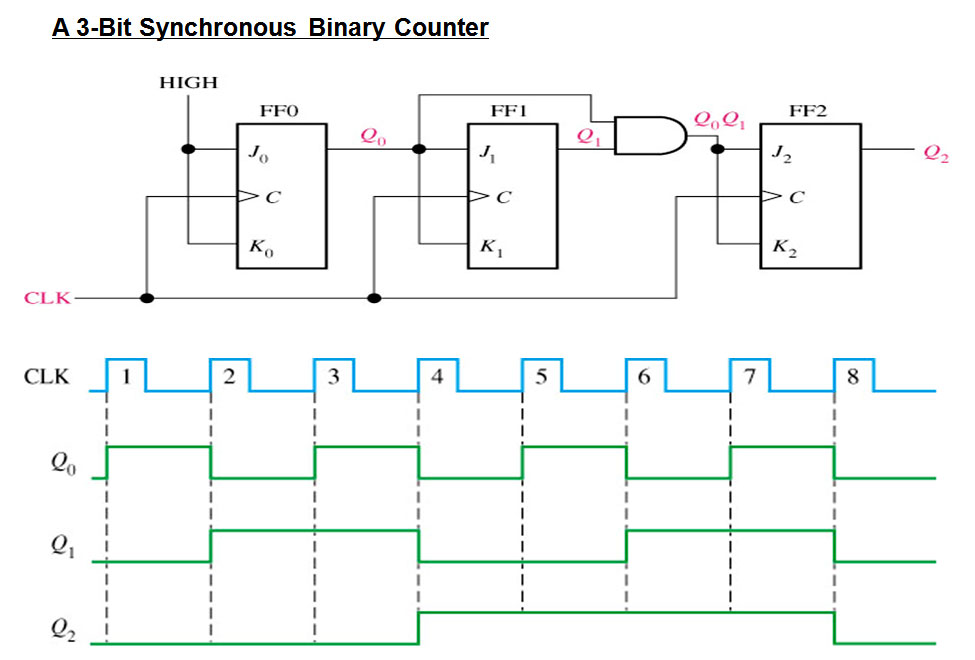
# Theory:

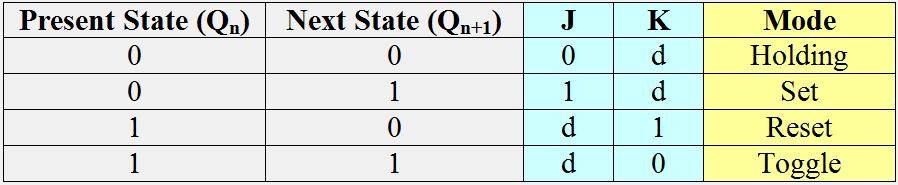
## SYNCHRONOUS COUNTER

Synchronous or Parallel counters are those in which all the flip flops are triggered simultaneously (in parallel) by clock input pulses. Since the input pulses are applied to all the flip flops, some means must be used to control when a flip flop is to toggle and when it is to remain unaffected by clock pulse.



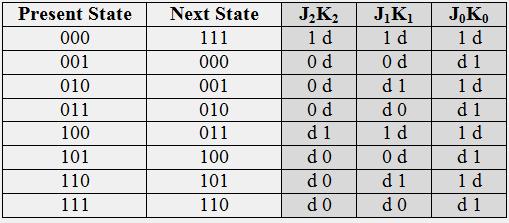
JK flip flop Characteristic Table





Excitation Table

Looking at the characteristic table and the excitation table we can make the state table and the corresponding excitation table. From which we make the K map of each JK input and them make the 3 bit synchronous UP counter circuit.

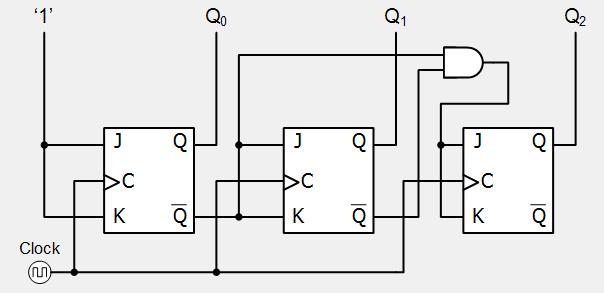


State Table and corresponding Excitation Table (d=don’t care)

Operation:

Flip flop 1 acts as toggle flip flop since J0 =K0 =1. Q0 output of FF-1 is applied to J1 as well as K1. Hence if Q0=1 at the instant of triggering, then FF-2 will not change its state. Q0 and Q1 are ANDed and the output of AND gate is applied to J2 and K2. Hence when Q0 and Q1 both are simultaneously high, then J2= K2=1 and FF-3 will toggle. Otherwise there is no change in the state of FF-3. So in general we can say that each FF should have its J and K inputs connected such that they are high only when the outputs of all lower order FFs are in the high state.

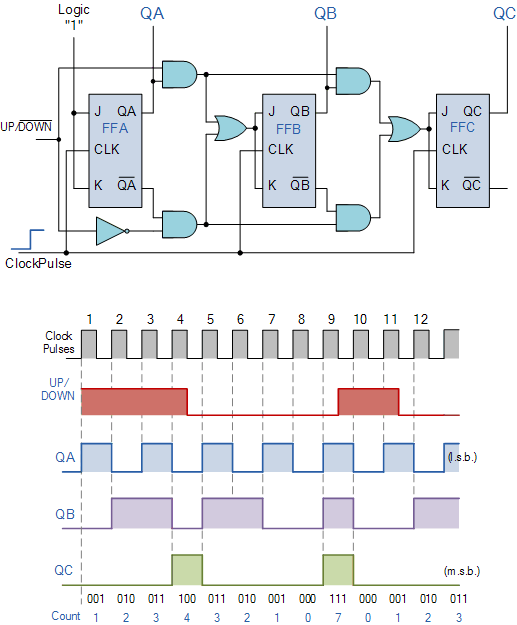
## A 3 bit synchronous DOWN counter:



The making and working of a synchronous DOWN counter is same as that of a UP counter. The only difference is from where the output is taken.

## A 3 bit synchronous UP /DOWN counter:

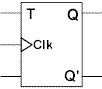
Both synchronous and asynchronous counters can count UP or DOWN, but there is another more Universal type of counter that can count in both directions either UP or DOWN depending on the state of their input control pin and these are known as Bidirectional Counter. Bidirectional counters, also known as UP/DOWN counters, can count in either direction through any given count sequence and they can be reversed at any point within their count sequence by using an additional control input as shown below.



The circuit above is of a simple 3 bit UP/DOWN synchronous counter using JK FFs configured to operate as toggle or T-type FFs giving a maximum count of zero (000) to seven (111) and back to zero again. The 3bit counter advances upward in sequence (0,1,2,3,4,5,6,7) or downwards in reverse sequence (7,6,5,4,3,2,1,0) but generally, bidirectional counters can be made to change their count direction at any point in the counting sequence. An additional input determines the direction of the count, either UP or DOWN and the timing diagram gives an example of the counters operation as this UP/DOWN input changes state.

Similarly, we can make synchronous counter using T FFs and D FFs.

## T flip flops:



In a T flip flop when the clock triggers, the value remembered by the flip flop either toggles or remains the same depending on whether the T input (*Toggle*) is 1 or 0.

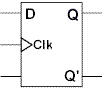
|  |  |
| --- | --- |
| **T** | **Q(next)** |
| 0 | Q |
| 1 | Q' |

**Truth Table of T flip flop**

|  |  |  |
| --- | --- | --- |
| **Q** | **Q(next)** | **T** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Excitation Table of T flip flop**

## D flip flops:



In a D When the clock triggers, the value remembered by the flip-flop becomes the value of the D input (Data) at that instant.

|  |  |
| --- | --- |
| **D** | **Q(next)** |
| 0 | 0 |
| 1 | 1 |

Truth Table of D flip flop

|  |  |  |
| --- | --- | --- |
| **Q** | **Q(next)** | **D** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Excitation Table of D flip flop

## Generalization of synchronous counters i.e n bit synchronous counter:

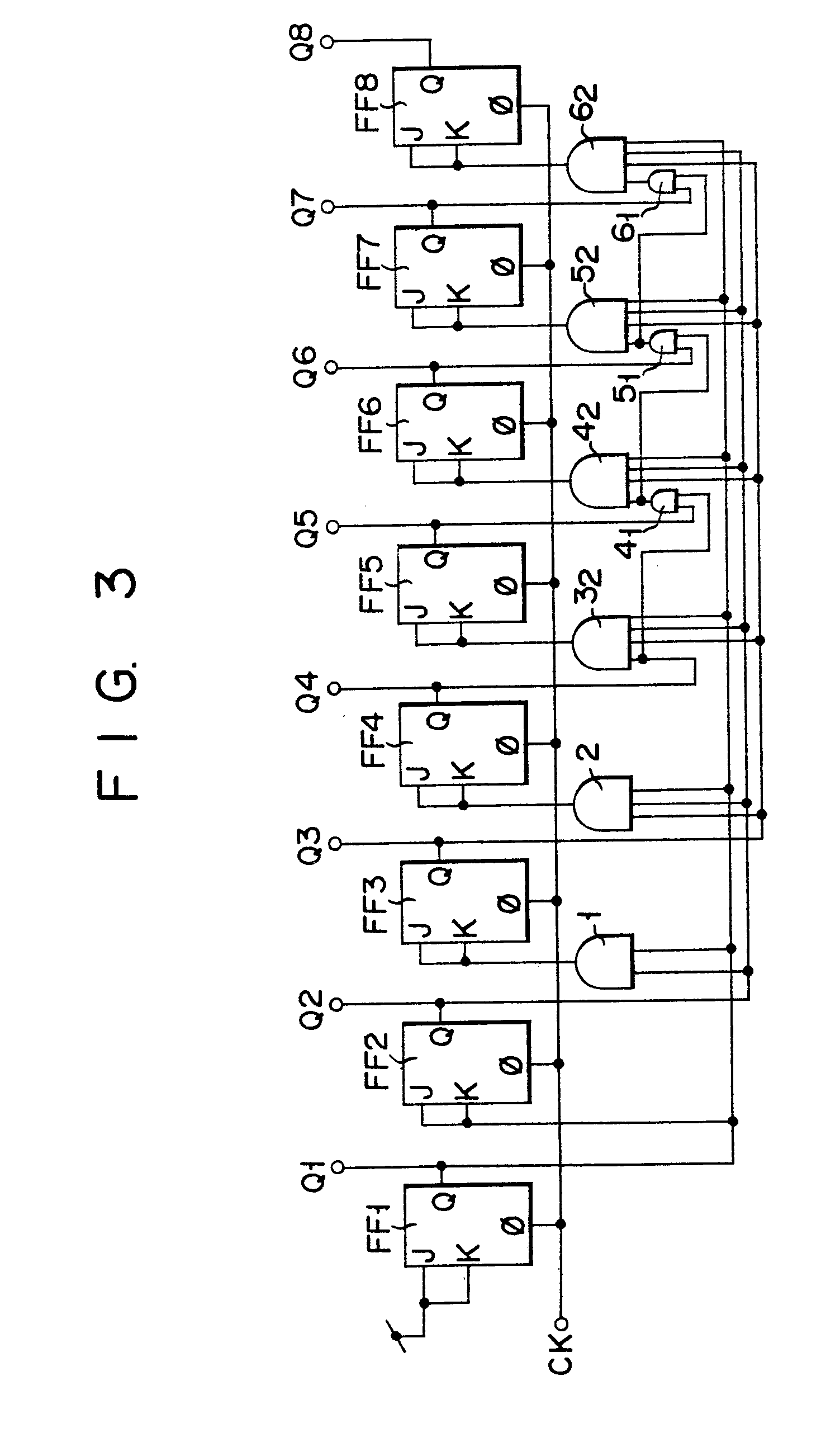
An *n*-bit counter has *n*-FFs with 2*n* distinct *states*, where each state corresponds to a

particular *count*. Accordingly, the possible *counts* of an *n*-bit counter are 0 to (2*n*-1). Moreover an n-bit counter has *n* output bits (Q*n-1* …. Q*2* Q*1* Q*0*).

After reaching the maximum count of (2*n*-1), the following clock pulse resets the count

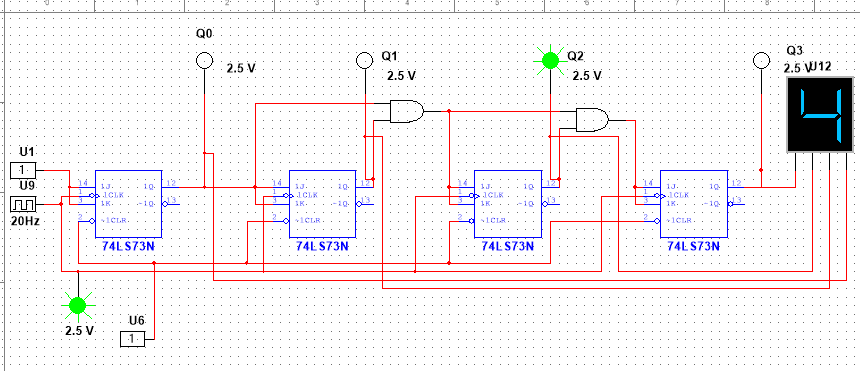
back to 0.

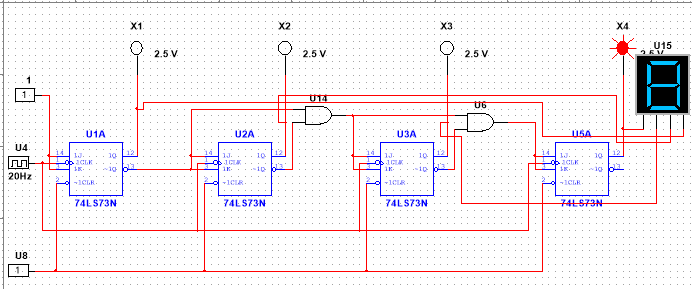
## Example: 8 bit synchronous UP counter



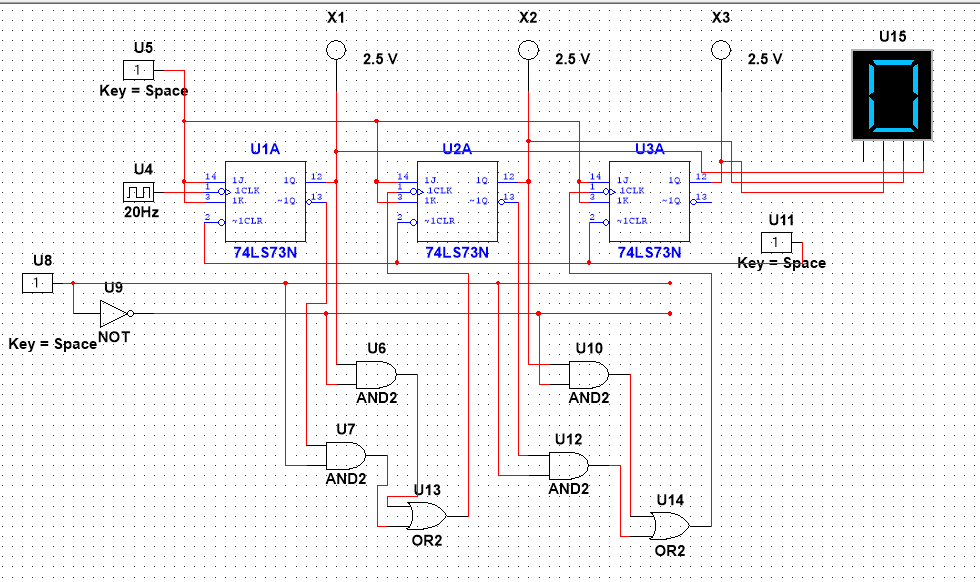
# Design:

## Synchronous UP counter

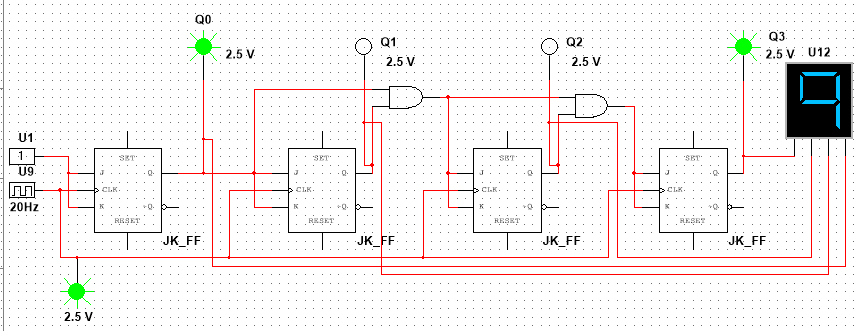
****

Synchronous DOWN counter****

## Synchronous UP DOWN counter

****

## Synchronous Decade Counter

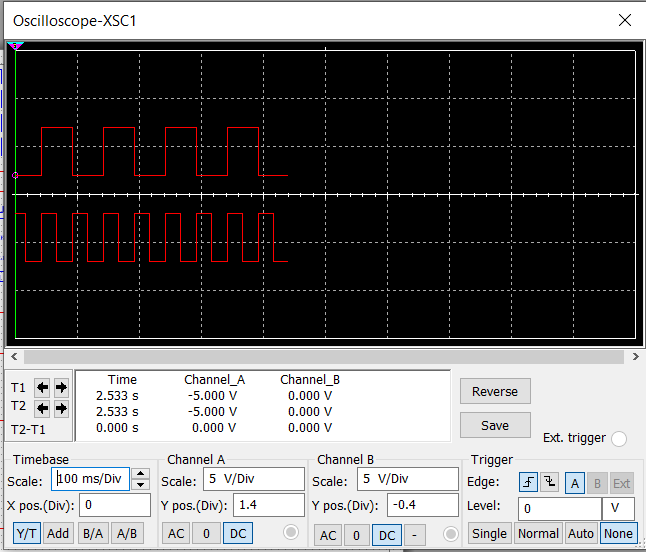
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# Procedure:

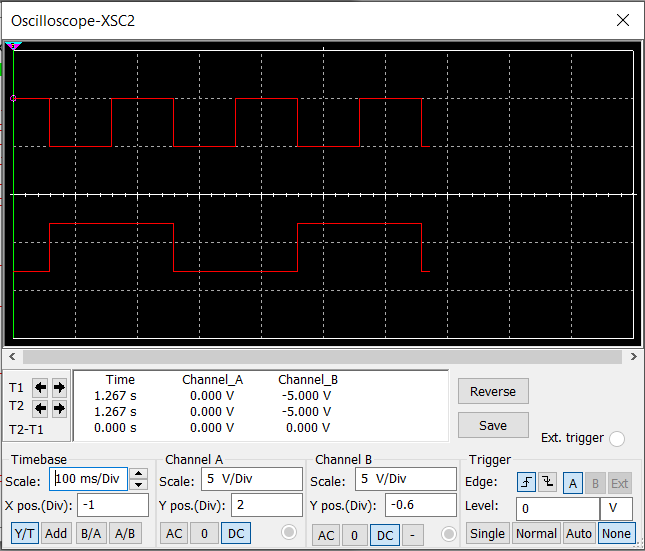
1. Connect the components as shown in the circuit diagram.
2. Give +5V supply to the IC’s.
3. From the LED observe the outputs and also observe the output on 7 Segment LED display.
4. Make a note of the truth tables in the observations.
5. Use DSO / Oscilloscope for observation of various outputs of FFs (timing parameters)
6. Verify the Counting sequence accordingly.

# Observations:

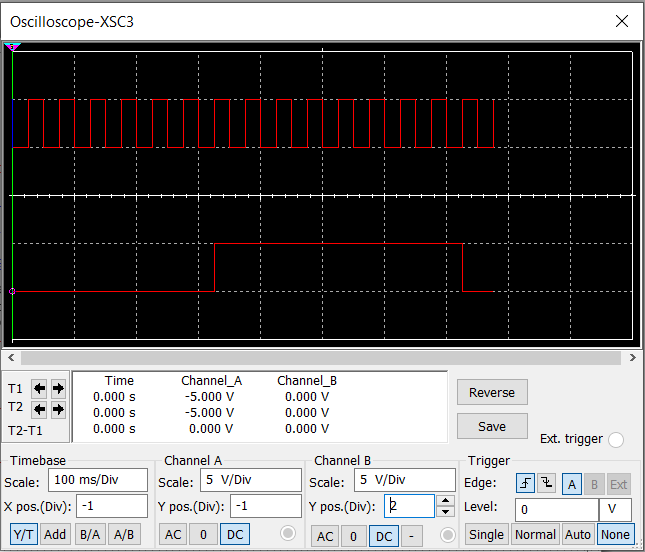
## Shows LSB (X1) and Clock respectively



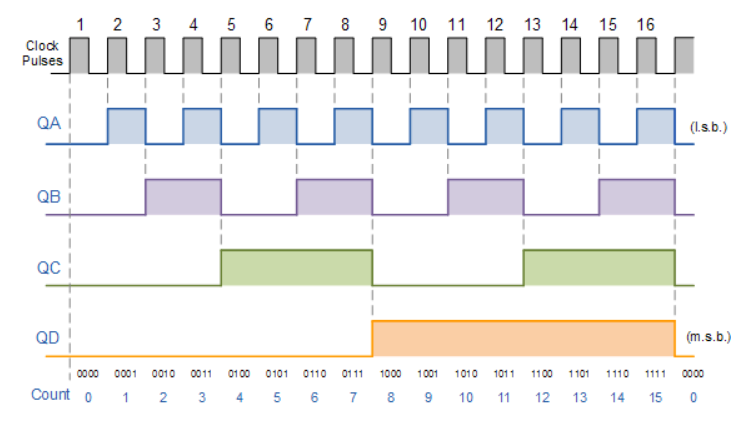
## Shows X2 X3 respectively



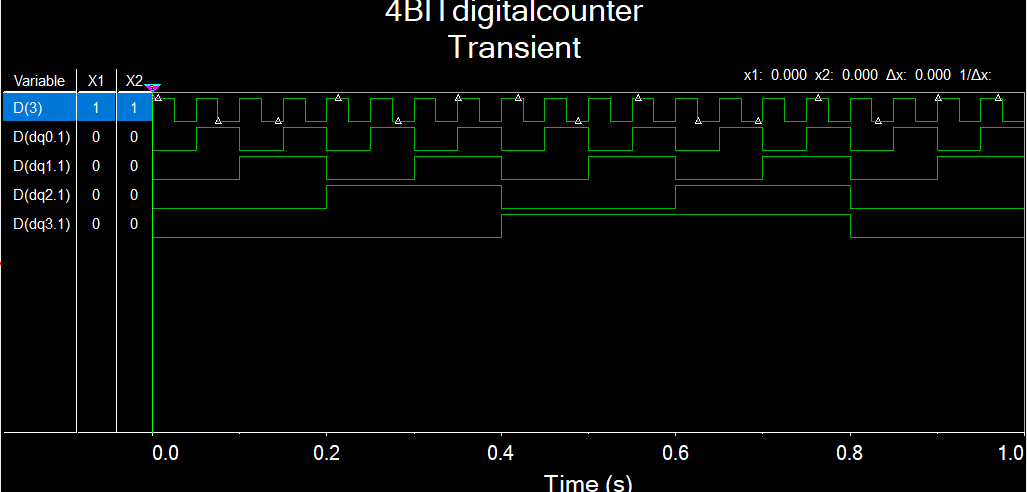
## Shows Clock and MSB (x4) respectively



## Expected waveforms.



## Observed output



# Result:

Above mentioned circuits were created and run in multisim software**.**

# Conclusion:

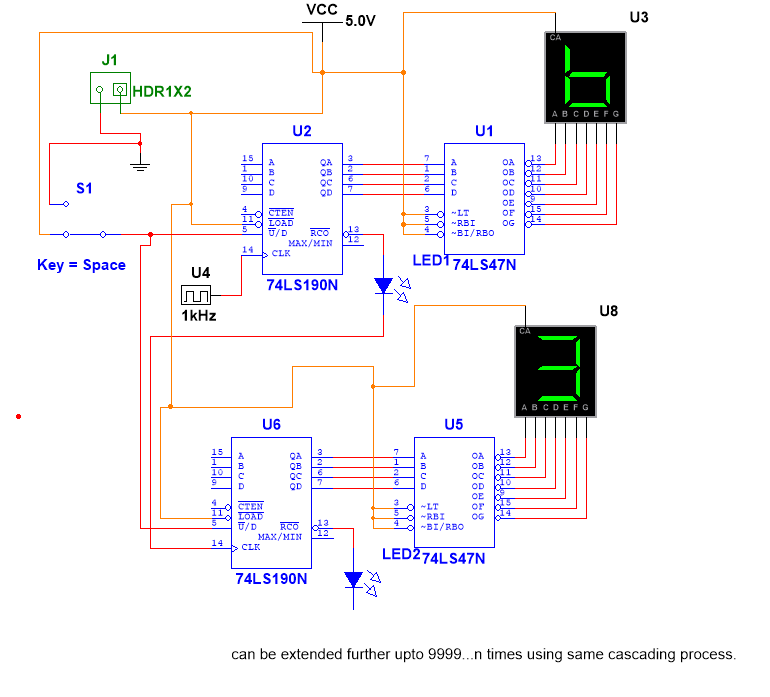
Truth tables were verified by simulating the created circuit.

# What did you learn?

I learnt how different synchronous counters are made, and I understood their working by simulating them and verifying the timing diagrams.

# Assignment:

## Created 0-99 up- down counter



Use switch s1 to change up or down mode.